COLECO INDUSTRIES INC.

DELTA GAME BOARD

REPAIR GUIDE

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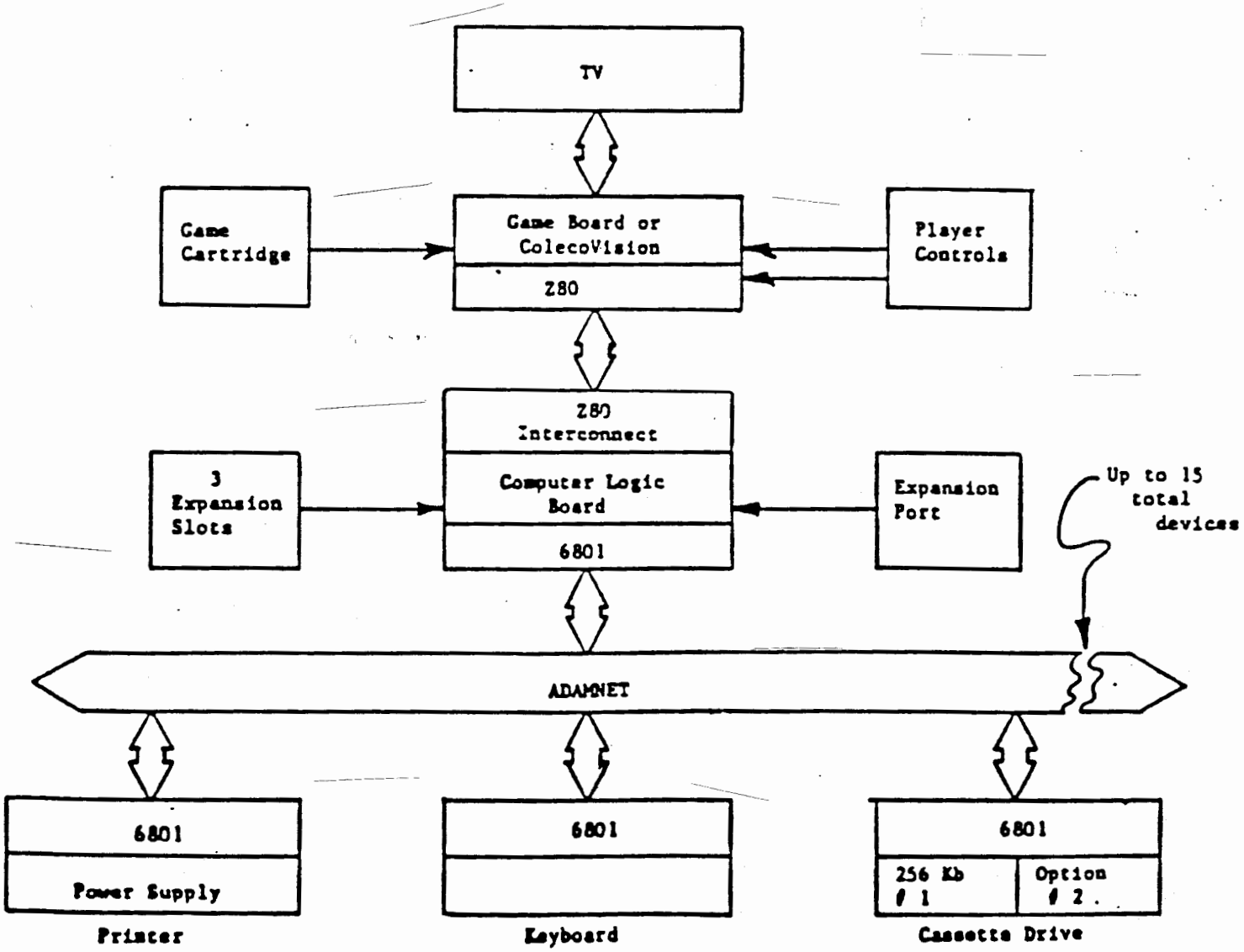
Chapter 1. ADAM COMPUTER SYSTEM BLOCK DIAGRAMS

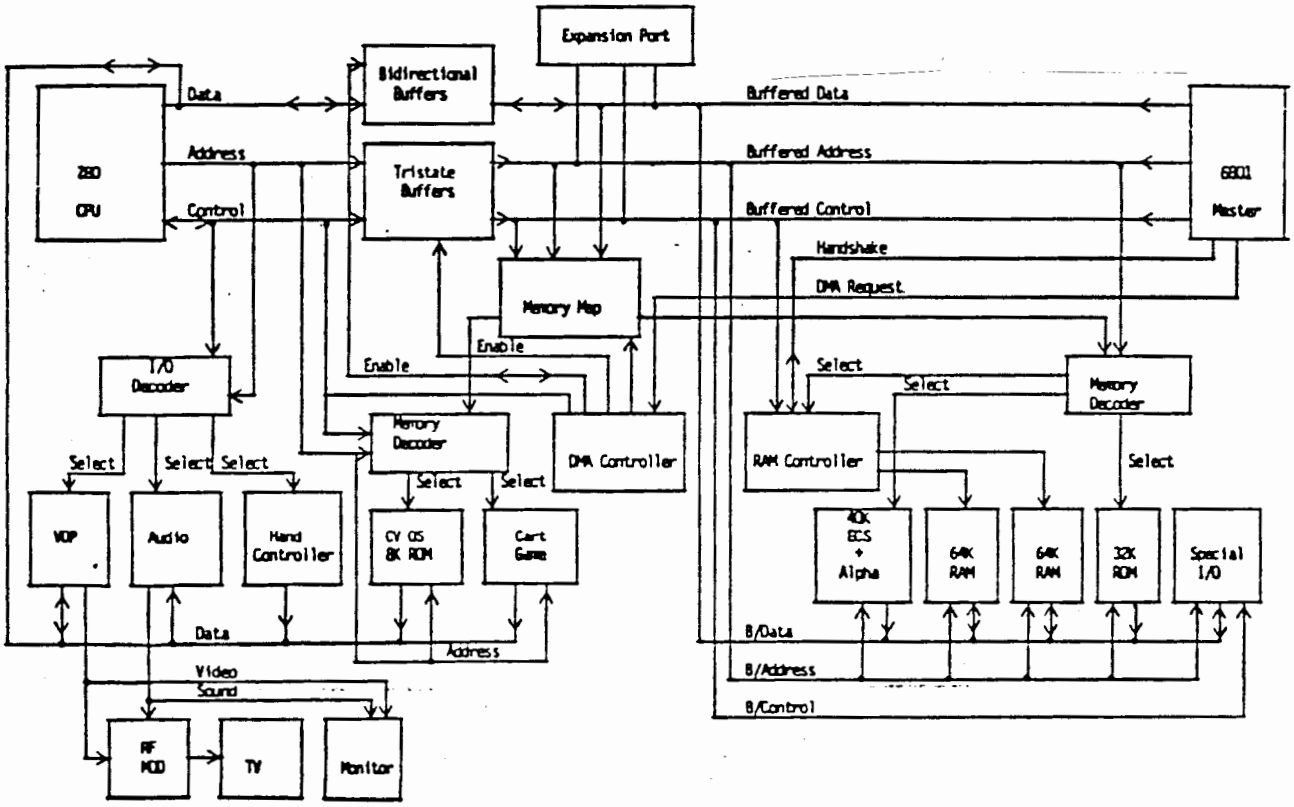
A. Complete System.

The Delta Game Board, combined with the Computer Logic Board and the AdamNet Communications Network make up the main computer system for the Adam Computer. The Computer Logic Board provides the operating system for the word processing and the DRAM used for programming operations. The Game board includes the Z80 Central Processing Unit, game operating system, and interfaces for the game cartridge ROM and hand controllers. (See Figure 1 below.)



B. Game & Logic Board.

The Game Board includes seven major systems: the Z80 CPU, Video Display Processor, Audio Generator, Radio Frequency Modulator, Clock Generation, Game Operating System/Cartridge ROM, and Game Controllers. The Adam Home Computer System, or the Game Board connected to the Computer Logic Board is shown functionally in Figure 2 below.



Chapter 2. HOW TO USE THIS GUIDE

A. Confirm / Verify Problems Described

1. Inspect for physical damage as most probable cause of failures.
   a. Check all connectors, wiring, and components for good connection.
   b. Clean edge fingers and other contact points.

2. Check Revision Level of PC Assembly. (Reference assembly drawing)
   a. 41580 - Delta Game PC Assembly.

B. Cautions.

1. Handle assemblies and components with care appropriate to avoid damage to static sensitive devices.

   a. Testing must be performed at an ESD protected work station.

      1. Conductive mat/work surface.

      2. Properly grounded operator.

      3. No plastic tools e.g. desoldering tools.

C. Equipment Necessary to perform tests herein described or referenced.

1. System Final Tester
2. Board Level System Tester
3. Known Good Adam Card Set
4. System Final Test Cartridge
5. CPU Burn-In cartridge
6. Game Board Final Test Cartridge
7. Expansion Module #1 (Atari) w/ game cartridge

D. Using Customer description of problem and/or previous test results (see Chapter 4: Quick Overall Check), use Symptom Index as diagnostic pointer to probable defects and cause.

CHAPTER 3. SYMPTOM INDEX

Symptoms below are listed in descending order of probability.

Symptom	Cause
Bad Video.	Defective U9. Defective U1. Defective U10. Defective U16. Defective Y1. Cold solder J4 Pin 5. U9 Pin 2 not thru PCB. R42 wrong value. Defective C62. Defective E14. Defective Q8. Defective Q3 RF Modulator PCB.
No audio/video	Defective U1. Defective Y1. Defective E28. Dirty fingers/interconnect Cable on Delta Game Bd. Defective U23 Audio jumper connector shorted to DIN plug. Broken trace E1. Dirty fingers/edgecard.
Controller port #1 defective.	D-Connector pin not soldered. 9 Pin D connector not soldered. Defective U6.

Symptom	Cause
No Audio/video exp. buss.	Broken audio jumper. Pin 31 shorted to gnd edge card.
No sound/power-up.	Blue and green wire shorted on CPU fan plug.
Cannot load tape.	Defective U1. Defective U2.
Reset Problem .	Defective U1. Defective U28.
Controller port #2 defective.	Shield ground braid shorting controller port
CPU Resets by itself.	Cold Solder Pin 1 & 2 U1.
Poor sound.	4.5 MHz misadjusted carrier.

Chapter 4. QUICK OVERALL CHECK

A. Check all system interconnections for integrity.

B. Check power supply voltages at all PC Assemblies.

C. Use System Final Tester to highlight functional problems. See Set-up drawing T-1800 and reference procedure: CPU (System Cartridge) Test, Log 106.1; Appendix A. Error code information is listed below:

Error messages:

1. Possible media failure - unsuccesstul attempt to access a block on tape during the first pass on the tape test.

2. Fail Aux. Video - Auxiliary video frequency and amplitude do not meet required limits. Tested at the auxiliary jack located at the rear of the ADAM cpu.

3. Failed controller port # - the state of each pin on the hand controller jacks is changed, sampled, and failed to be at expected level.

4. Controller port interaction - changes at pins of one hand controller port modify the state of the other port.

5. Read or Write drive fail - unsuccessful attempt to read or write to a tape drive, probably due to inability to access a block.

6. Xfer drive fail - data read from drive under test fails to compare to the data written.

7. Rom Fail - The computed ROM checksums do not compare and the computed values are printed to the screen.

Error messages continued....

8. Lower / upper 32K RAM failure - pattern testing on the system ram failed.

9. Can't sync up with master - communications between the Z80 and the network master 6801 were unsuccessful.

10. Drive 2 or aux. net fail - the signals at the drive two connector were determined to b bad or missing or the aux. network connector signals were not present.

D. Use Game board system level test procedure, Log 158.0, Appendix D, for additional performance evaluation.

E. Expansion Module #1 (Atari game cartridge interface) may be used to check game board performance and interconnects through the Logic Board. Insert module into expansion port and test for proper game operation.

	Computer Mode OPTIONS Game Mode			
64K DRAM	1	2	3	4
Lower 32K Choices	32K Boot ROM	32K RAM1	32K RAM2 (SLOT)	8K ColecoVision Operating System 24K RAM1
Upper 32K Choices	32K RAM1	32K AUX ROM (SLOT)	32K RAM2 (SLOT)	32K EXT. ROM GAME CARTRIDGE

CHAPTER 5. TEST FIXTURES

A. System Final Test documentation.

1. T-1638 Rev A: System Final Test Assy.
2. T-1132 Rev A: System Test Hardware Sub-Assy.
3. T-1132 Rev A: System Test Hardware Schematic.
4. Log # 106.1 : CPU (System Cartridge) Test Procedure.
5. T-1614 Rev B: System Test Interfacing Harness.
6. T-1619 Rev 0: Interface Harness Wire List.
7. System Test Cartridge Rev 3.1.
8. T-1800: Test Set-Up Drawing.

B. Board level system test documentation.

1. T-1721 Rev A: Board Level System Test Interconnection Diagram.
2. T-1794 Rev 0: Board Level System Test Interface Harness.
3. T-1797 Rev 0: Interface Harness Wire List.
4. Log #158.0 Delta Game PCB Repair Test Procedure.
5. System Test Cartridge Rev 3.1.
6. CPU Burn-In Cartridge. Rev 5.0.
7. Delta Game Final Test Cartridge. Rev 1.0.

CHAPTER 6. SCHEMATIC & ASSEMBLY DOCUMENTATION

GAME BOARD

Delta Game Assembly: 41580

Delta Game Logic: 41844

ADDITIONAL DRAWINGS

Delta Logic Assembly:	41581D
Gamma Logic Assembly:	41079D
Gamma/Delta Schematic:	41843
Interconnect Board Assembly:	41571
Interconnect Board Schematic:	41840
Power Supply Assembly:	41240
Power Supply Schematic:	41234

APPENDIX B. FUNCTIONAL SUB-BLOCK DESCRIPTION

Note: Reference Board Assemblies and Schematics for component identification.

1. Z80 CENTRAL PROCESSING UNIT (CPU) - "U1"

The Z80 is the controlling CPU of the Adam Home Computer System with responsibilities to both the Data Game Board and Computer Logic Board. The Z80 initializes the Adam system in one of two modes: the game mode or the computer mode. The mode of operation, determined by the memory map, is dependent on which reset switch has been activated. (At power on, the default condition is computer mode.) The Z80 CPU is capable of configuring the memory map, shown in Figure 3 below, into any conbination of lower and upper memory and switching between them.

Z80 Central Processing Unit (CPU) Continued...

An M1 wait request hardware is included on the Delta Game Board (1/2 of U8) that enables the Z80 to automatically introduce one clock period to the memory fetch cycle.

Memory timing requirements are as follows:

a. Access time from chip select to data output valid -- 375 ns max.

b. Access time from address valid to data output valid -- 510 ns max.

2. VIDEO DISPLAY PROCESSOR (VDP) - "U9"

The video display is generated by the TI 9928 which directly outputs video R-Y, B-Y, Y signals to the RF circuitry on the Game board. The TI 9928 uses a table driven architecture that allows the programmer to control every pixel in the visual display area. It also allows the programmer to define and control 32 objects or "sprites" which may be placed anywhere on the display and moved around at will. The VDP chip is addressable in DATA MODE, used whenever VRAM is being written or read; and in REGISTER MODE, used when control information is being written to and read from one of the chip's internal registers. The addresses of these ports in the CPU I/O address space are as follows:

a. Data Port....0BEH.

b. Register Port....0BFH.

Video Display Processor, continued....

The VDP is driven by a 10.7 MHz clock (see paragraph 5b). Because the VDP is sensitive to noise at the clock, and LC filter circuit has been added to the Vcc supply line for the clock circuit to eliminate the audio interference on video. Since the VDP has 10.7 MHz clock, the access time for the VRAM is 200 ns maximum.

3. AUDIO GENERATOR - "U20"

Sound is produced by the TI 76489 sound generator controller. The chip contains three programmable tone generators, a programmable white-noise generator, and programmable attenuation for each of the channels. The chip is addressed through a single port, at location 0FFH. Audio output is 450 mV @ 2mA, 0dB attenuation; quiescent output is 2.0 Vdc. Wait-request hardware has been included in the system because the sound chip is slow peripheral requiring data lines to be stable for a relatively long time while writing to it.

4. RADIO FREQUENCY (RF) MODULATOR - "U21"

The RF section utilizes an NS 1889 chip to interface audio, color difference and luminance signals to the antenna terminals of a TV receiver. It includes two VHF channels, 3 or 4, selectable by a slide switch with determined LC tank circuits. The chroma subcarrier oscillation is obtained from the 3.58 MHz system clock to ensure accuracy and stability. The frequency modulator of the sound oscillator is achieved by using a 4.5 MHz tank circuit and deviating the center frequency via a varactor diode. Due to the incompatible signal level between the VDP 9928 and the 1889, a DC restoration circuit has been added to ensure the DC level of the video signal.

5. CLOCK GENERATION - "Q7, U22, U8, Q2, Q8"

Three clocks are included on the Delta Game Board: the System Clock, the Video Chip Clock, and the 7.1 MHz Clock.

a. The System Clock is a 3.58 MHz square wave generated by dividing the 7.1 MHz clock by two. The output of the divider stage has a dynamic pullup to ensure fast rise times and a valid logic one to the Z80.

b. The Video Display Processor is driven at pin 40 by the Video Chip Clock (10.7 MHz) which is obtained from the third multiple, high Q tuned tank circuit on the 3.58 MHz system clock at U8, pin 9.

c. The 7.1 MHz is generated by a crystal controlled oscillator. The output of the oscillator circuit is buffered and divided by two (1/2 of U8) in order to provide a 50% duty cycle waveform.

6. OPERATING SYSTEM/CARTRIDGE ROM

The Game Board system includes an 8K byte operating system ROM (U2) and a connector (J1) for cartridge ROM up to 32K byte memory. These memories are directly addressable by the Z80 CPU. Locations of these memory blocks are as follows:

a. Cartridge ROM 8000H --- FFFFH

b. Operating System ROM 0 --- 1FFFH

7. GAME CONTROLLERS

Two game controllers, identical to those provided with ColecoVision, are provided with the Adam System. Each controller includes an 8 position joystick, two reaction keys called Fire and Arm, and a 12-key numeric keypad.

Connected to the Delta Game Board via two "D" type connectors (J5 & J6), each controller is accessed by the system through it own port. The addresses of these ports in the system I/O are as follows:

a. Controller #1 0FCH

b. Controller #2 0FFH

For each controller, 18 switches are read on a single 8-bit port. Therefore, once a port has been read, some decoding is required to determine which switches have been depressed. The layout and the encoding of the various controller functions are shown in Figure 4. Two spinner switches, not wired in the controller, are used in games such as Turbo. To ensure that the spinner switch closures are processed as soon as they occur, the closures are connected to the CPU maskable interrupt, and the cartridge software determines which switch will cause the interrupt.

APPENDIX C. ANNOTATED SCHEMATIC

Reference Schematic #41844

Circuit Node		Comment
A.	+5V	
B.	+12V	
C.	-5V	
D.	System Clock	@U8 - 11, 7.16 MHz
E.	Z80 Clock	@U8 - 9, 3.58 MHz
F.	Audio Clock	@U2 - 14, 3.58 MHz
G.	VDP Clock	@U22 - 4, 10.7 MHz
H.	Z80 Reset	Active low in response to Game Reset Switch.
I.	A0 - A15	Z80 Address buss, active.
J.	D0 - D7	Data lines, active.
K.	AD1 - AD7	Video Ram Address buss, active.